09/848,718

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Terms	Documents
L3 and (etch near2 stop)	7

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DATE: Friday, September 06, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	L3 and (etch near2 stop)	7	L4
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L1	(field adj effect adj transistor) or fet	63621	L1

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Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 6441418 B1

L4: Entry 1 of 7 File: USPT Aug 27, 2002

US-PAT-NO: 6441418
DOCUMENT-IDENTIFIER: US 6441418 B1

TITLE: Spacer narrowed, dual width contact for charge gain reduction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6429477 B1

L4: Entry 2 of 7 File: USPT Aug 6, 2002

US-PAT-NO: 6429477
DOCUMENT-IDENTIFIER: US 6429477 B1

TITLE: Shared body and diffusion contact structure and method for fabricating same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6380039 B2

L4: Entry 3 of 7 File: USPT Apr 30, 2002

US-PAT-NO: 6380039
DOCUMENT-IDENTIFIER: US 6380039 B2

TITLE: Method for forming a FET having L-shaped insulating spacers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 4. Document ID: US 6313003 B1

L4: Entry 4 of 7 File: USPT Nov 6, 2001

US-PAT-NO: 6313003
DOCUMENT-IDENTIFIER: US 6313003 B1

TITLE: Fabrication process for metal-insulator-metal capacitor with low gate resistance

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 5. Document ID: US 6174794 B1

L4: Entry 5 of 7 File: USPT Jan 16, 2001

US-PAT-NO: 6174794
DOCUMENT-IDENTIFIER: US 6174794 B1

TITLE: Method of making high performance MOSFET with polished gate and source/drain feature

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 6. Document ID: US 4811078 A

L4: Entry 6 of 7 File: USPT Mar 7, 1989

US-PAT-NO: 4811078
DOCUMENT-IDENTIFIER: US 4811078 A

TITLE: Integrated circuit device and process with tin capacitors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 7. Document ID: US 4811076 A

L4: Entry 7 of 7 File: USPT Mar 7, 1989

US-PAT-NO: 4811076
DOCUMENT-IDENTIFIER: US 4811076 A

TITLE: Device and process with doubled capacitors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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Terms	Documents
L3 and (etch near2 stop)	7

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Previous Page Next Page